REMARKS

Reconsideration and withdrawal of the rejections of the application are respectfully requested in view of the foregoing amendments and following remarks.

I. STATUS OF THE CLAIMS AND FORMAL MATTERS

The Office Action indicates that claims 1-5 and 14-16 are pending in this application. Claims 1 and 14 are in independent form. By this amendment, each of the pending claims is amended for additional clarity, and new dependent claim 26 is presented for consideration on the merits. Upon entry of this amendment, claims 1-5, 14-16, and 26 are pending. No new matter has been added. It is submitted that the claims, as originally presented, were in full compliance with the requirements of 35 U.S.C. §112. Changes to claims are not made for the purpose of patentability within the meaning of 35 U.S.C. §101, §102, §103, or §112. Rather, these changes are primarily directed to form and are made simply for clarification.

II. REJECTIONS UNDER 35 USC § 112

The Office Action rejects claims 1-5 and 14-16 under 35 USC § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. More specifically, the Office Action identifies specific terms in claims 1, 4, 5, 14, and 15 as being indefinite. While Applicant respectfully maintains that the original claims are not indefinite and satisfy the requirements of § 112, ¶ 2, Applicant has herein amended these claims for additional clarity, and respectfully submits that the rejections under 35 USC § 112, ¶ 2 have been obviated and rendered moot and should thus be withdrawn.

II. REJECTIONS UNDER 35 USC § 103(a)

The Office Action states that claims 1, 3-5 and 14-16 are rejected under 35 USC § 103(a) as being unpatentable over *Computer Organization & Design The Hardware/Software Interface* to Patterson et al. (hereinafter, "Patterson") in view of *8051 Tutorial: Addressing Modes;* Vault Information Services, 2001, (hereinafter, "Vault"). The Office Action also states that claim 4 is rejected under 35 USC § 103(a) as being unpatentable over Patterson in view of Vault and common knowledge in the art, with the Examiner taking Official Notice that the claim limitations stated in claim 4 were commonly known in the art at the time of the invention.

As an initial matter, Applicant respectfully notes that the reasoning set forth in the Office Action for rejecting claim 4 *does not* rely on Patterson in view of Vault *without* Official Notice as to alleged common knowledge in the art; however, such grounds are set forth with respect to claim 2. In any case, Applicant respectfully traverses the Official Notice taken by the Examiner at least insofar as Applicant respectfully submits that it was not well known at the time of the invention to provide the combination required by claim 4 as a programmable logic device on an identical semiconductor chip and having register-to-register addressing functionality. Accordingly, in accordance with 37 CFR § 1.104(c)(2), Applicant respectfully requests that the Examiner provide an affidavit or documentary evidence to support such factual assertions if the rejection is to be maintained on these grounds.

As understood by Applicants, Patterson relates to a MIPS architecture having an ALU, a data memory, registers coupled to the ALU input, an instruction memory, and a program counter (PC).

As understood by Applicants, Vault relates to an 8051 instruction set that includes indirect addressing, allowing for extra bytes of Internal RAM found on an 8052 to be accessed. In executing such an indirect addressing instruction, the 8051 analyzes the value of the R0 register, and loads the accumulator with the value held in the Internal RAM location addressed by the value of the R0 register.

Claim 1 recites, *inter alia*:

> An operation-processing device for performing operation processing based on an arbitrary operation program, said device comprising:
>
> ***a register array*** having a plurality of registers each for holding an arbitrary value based on a write address and a write control signal and ***outputting the held value to a signal line based on a read address***;
>
> ***an operation portion having an input coupled to said signal line, the operation portion being operable for performing an operation on a value read from said register array to said signal line;***
>
> an instruction-decoding portion for decoding an operation instruction from an operation program for operating said operation portion; and
>
> an instruction-execution-controlling portion for controlling said register array and the operation portion in order to execute an operation instruction decoded by said instruction-decoding portion,
>
> ***wherein said instruction-execution-controlling portion selects one of said registers based on said operation instruction; and***
>
> ***wherein based on a value held by said selected register, said instruction-execution-controlling portion performs register-to-register addressing processing for selecting another of said registers of said register array.***

Applicant respectfully submits that Patterson and Vault, individually or in combination, do not teach or suggest the above combination of features recited in claim 1. More

specifically, Patterson and Vault do not teach or suggest, *inter alia*, "a register array having a plurality of registers each for . . . *outputting the held value to a signal line based on a read address; an operation portion having an input coupled to said signal line* . . . [and] being operable for performing an operation on a value read from said register array to said signal line . . . and an instruction-execution-controlling portion . . . [that] selects one of said registers . . . [and] based on a value held by said selected register . . . performs register-to-register addressing processing for selecting another of said registers *of said register array*." For example, in contrast to Applicant's claimed invention, neither Patterson nor Vault discusses register-to-register addressing in a register array as claimed (claim 1) at least insofar as (i) Patterson does not teach or suggest that a value stored in a given one of the registers coupled to the ALU may be used to address another of the registers coupled to the ALU, and (ii) Vault merely discusses indirect addressing with respect to moving data *from RAM to* an Accumulator register.

Therefore, Applicant respectfully submits that claim 1 is patentable.

Claim 14 recites, *inter alia*:

> An operation-processing method for performing operation processing based on an arbitrary operation program, said method comprising:
>
> accessing ***a register array*** having a plurality of registers, each for holding an arbitrary value based on a write address and a write control signal and ***outputting the held value to an input of an operation portion based on a read address***;
>
> decoding an operation instruction from said operation program;
>
> ***selecting one of said registers*** based on said operation instruction;

performing register-to-register addressing processing for selecting, based on a value held by said selected register, another of said registers of said register array; and

performing with said operation portion an operation on a value held by said selected another register.

Based on reasoning similar to that presented above with respect to claim 1, Applicant respectfully submits that the above combination of features recited in independent claim 14 are neither taught nor suggested by Patterson and Vault, individually or in combination, and thus claim 14 is also patentable.

Each of the other claims in this application is dependent on an independent claim discussed above, and is therefore believed patentable for at least the same reasons presented for the independent claim upon which it depends. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual reconsideration of the patentability of each on its own merits is respectfully requested.

CONCLUSION

In view of the above, it is submitted that all pending claims are patentable and the application is in condition for allowance, and Applicant respectfully requests early reconsideration and allowance of the application.

Applicant gratefully acknowledges the Examiner's consideration of this matter, and the Examiner is respectfully invited to contact Applicant's undersigned representative by telephone on any outstanding issue regarding the application.

Respectfully submitted,

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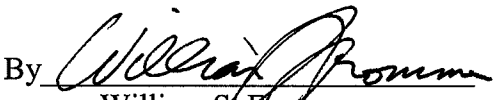
Attorneys for Applicants

By 
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